ABSTRACT OF THE DISCLOSURE

A lock detecting circuit is disclosed that detects whether a PLL circuit is in a locked state based on a phase difference signal supplied from a phase comparator of the PLL circuit, the lock detecting circuit comprising a first circuit that outputs a control signal having one level when the phase difference signal does not indicate a generation of a phase difference, and the other level when the phase difference signal indicates a generation of a phase difference; a second circuit that latches the control signal; and a third circuit that outputs, for a predetermined second term, a lock detecting signal indicating that the PLL circuit is in a locked state, when the latched control signal indicates the one level for a predetermined first term.